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United States Patent [19]
Rountree et al.
[11] Patent Number: 4,692,781
[45] Date of Patent: Sep. 8, 1987

[54] **SEMICONDUCTOR DEVICE WITH ELECTROSTATIC DISCHARGE PROTECTION**

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[21] Appl. No.: **617,876**

[22] Filed: **Jun. 6, 1984**

[51] **Int. Cl.**[4] **H01L 27/04;** H01L 29/78

[52] **U.S. Cl.** **357/23.13;** 357/41; 357/68

[58] **Field of Search** 357/23.11, 23.13, 84, 357/53, 41, 65, 68; 361/1, 56, 91

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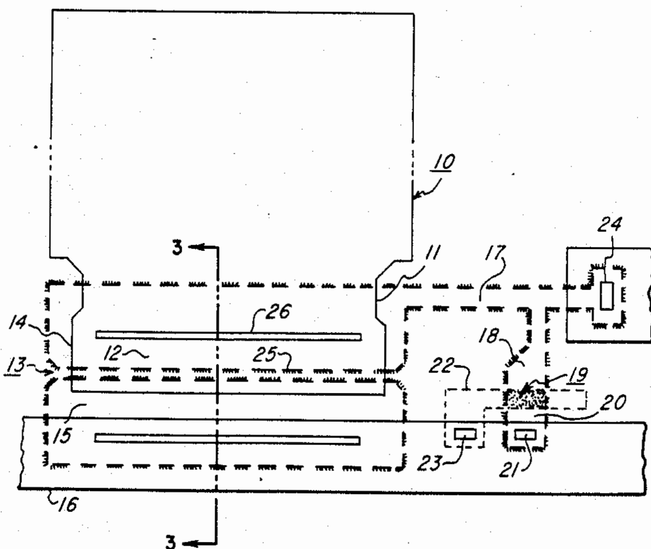
[57] **ABSTRACT**

An input protection circuit for an MOS device uses a thick-oxide transistor connected as a diode between a metal bonding pad and ground. The channel width of this transistor is chosen to be sufficient to withstand large, short-duration current spikes caused by electrostatic discharge. More important, the spacing between a metal-to-silicon contact to the drain of this transistor and the channel of the transistor (where heat is generated), is chosen to be much larger than usual so the metal of the contact will not be melted by heat propagating along the silicon surface during the current spike due to ESD. This spacing feature also applies to circuits for output pads, or circuits using diode protection devices.

10 Claims, 6 Drawing Figures



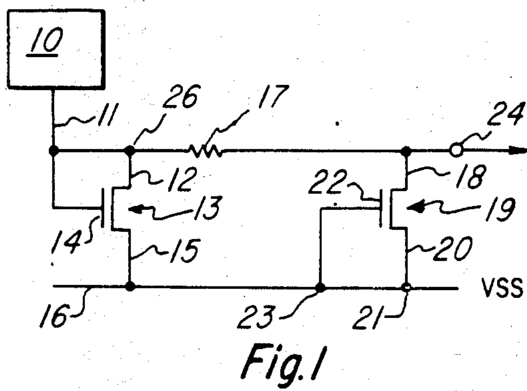


Fig. 1

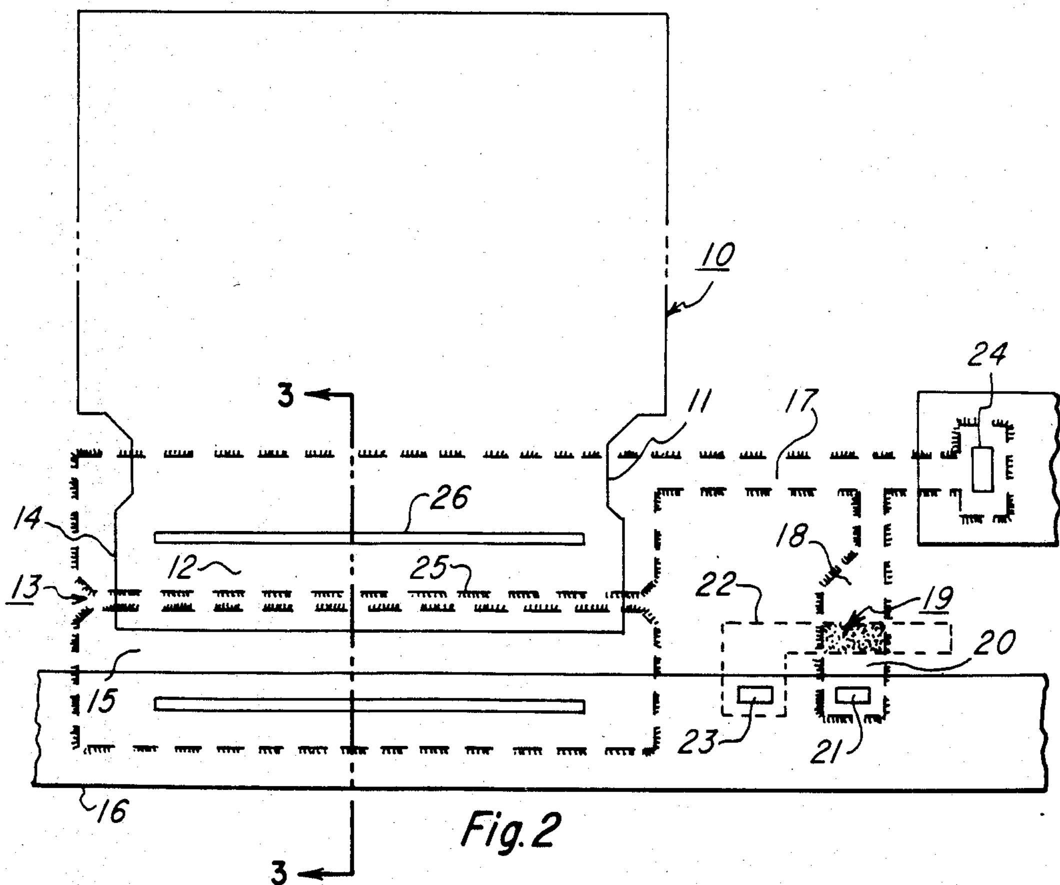


Fig. 2

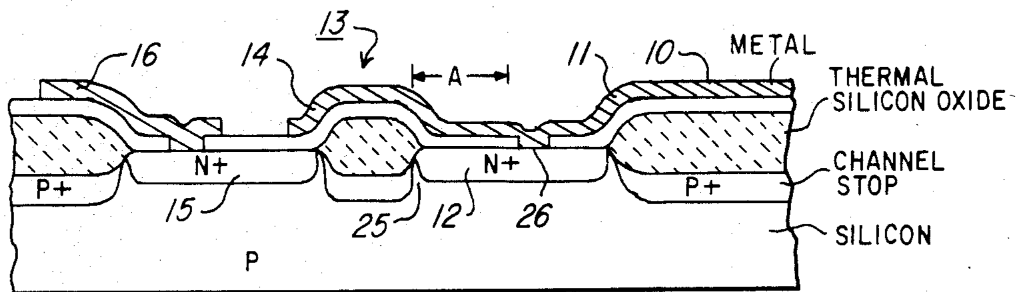


Fig. 3

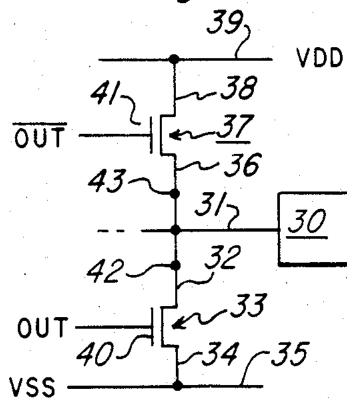


Fig. 4

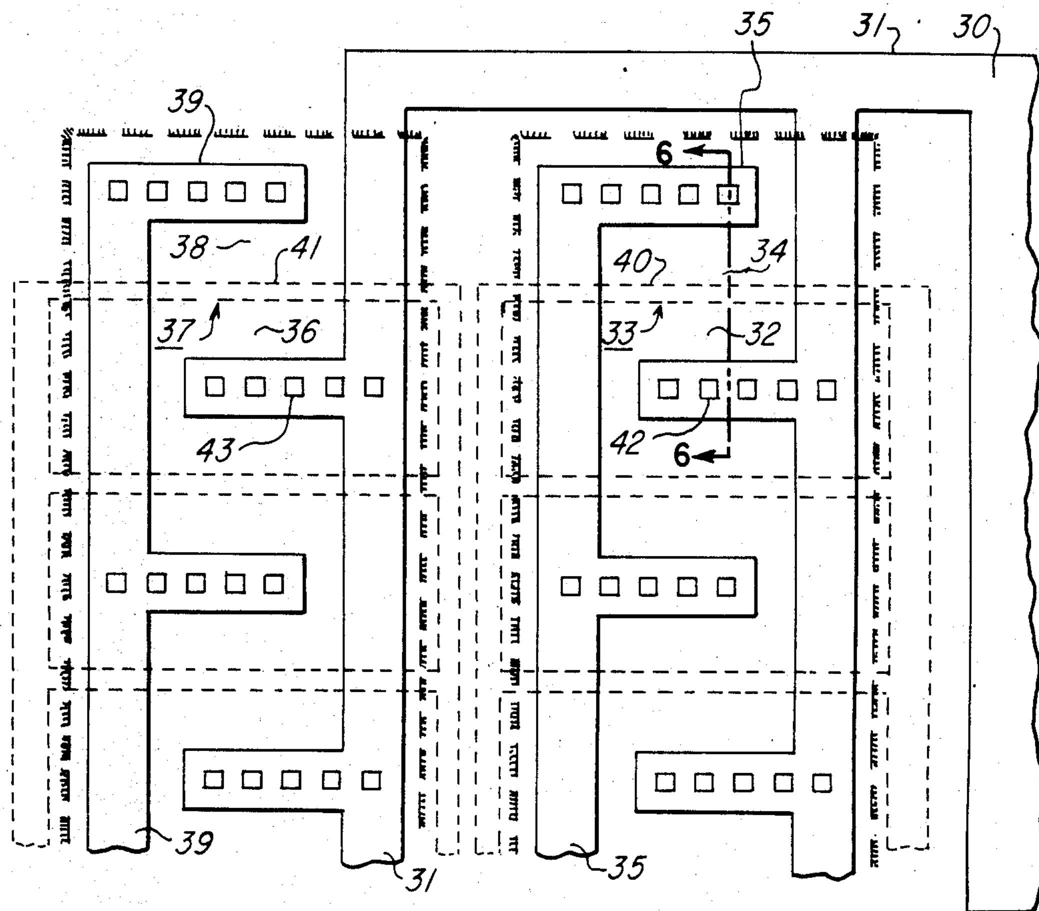


Fig. 5

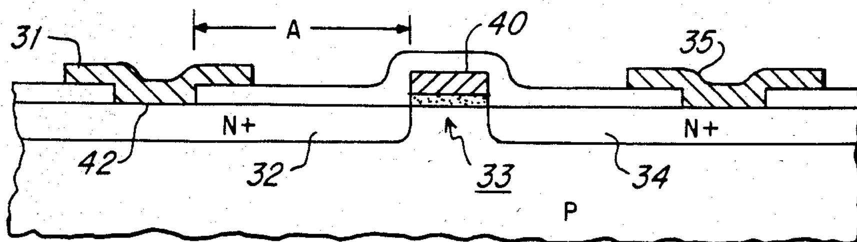


Fig. 6

SEMICONDUCTOR DEVICE WITH ELECTROSTATIC DISCHARGE PROTECTION

BACKGROUND OF THE INVENTION

This invention relates to semiconductor devices, and more particularly to electrostatic discharge protection circuits for input and output terminals of such devices.

All MOS devices employ protection circuits at the input and output pads to prevent damage to the internal circuitry caused by electrostatic discharge. Usually the voltage level which these protection circuits will withstand is about 3000 volts. An MOS device can be damaged by routine handling, even with this degree of protection.

It is the principal object of this invention to provide improved electrostatic discharge protection for MOS integrated circuits. Another object is to provide input and output protection circuits for MOS device that can withstand much more than 3000 volts ESD, preferably up to 8000 to 10000 volts.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the invention, an input protection circuit for an MOS device uses a thick-oxide transistor connected between a metal bonding pad and ground. The channel width of this transistor is chosen to be sufficient to withstand large, short-duration current spikes caused by electrostatic discharge. More important, the spacing between a metal-to-silicon contact to the drain of this transistor and the channel of the transistor (where most of the heat is generated), is chosen to be much larger than usual so the metal of the contact will not be melted by heat propagating along the silicon surface during the current spike due to ESD. This spacing feature also applies to circuits for output pads, or circuits using diode protection devices.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description which follows, read in conjunctin with the accompanying drawings, wherein:

FIG. 1 is an electrical schematic diagram of an input protection circuit according to the invention;

FIG. 2 is a plan view, greatly enlarged, of a part of a semiconductor chip having the circuit of FIG. 1;

FIG. 3 is an elevation view in section of the device of FIG. 2, taken along the line 3—3 in FIG. 2;

FIG. 4 is an electrical schematic diagram of an output circuit according to another embodiment of the invention;

FIG. 5 is a plan view, greatly enlarged, of a part of a semiconductor chip having the circuit of FIG. 4;

FIG. 6 is an elevation view in section of the device of FIG. 5, taken along the line 6—6 in FIG. 5.

DETAILED DESCRIPTION OF THE SPECIFIC EMBODIMENT

Referring to FIGS. 1, 2 and 3, an input circuit for an MOS device has a metal bonding pad 10 which is connected by a metal conductor 11 to the drain 12 of transistor 13. This transistor has its gate 14 shorted to its drain and has its source 15 connected to a Vss line 16. When the pad 10 is positive with respect to Vss, transistor 13 enters a low impedance state caused by secondary breakdown and conducts heavily to Vss, if pad 10 is positive with respect to Vss at a voltage level which exceeds the thick-oxide threshold voltage Vt level of about +20 or +25 v with respect to Vss. When the pad 10 is negative with respect to Vss, the N+ drain region 12 acts as a forward-biased diode and conducts heavily to Vss. The drain node 12 of transistor 13 is also connected to one end of elongated N+ path 17 which functions as a resistor, and the other end of the resistor is connected to the drain 18 of an MOS transistor 19 which functions as a "field plate diode". The source 20 of this transistor 19 is connected to the Vss line 16 at a metal to silicon contact 21, and the gate 22 (in this case polysilicon) is also connected to the Vss line 16 at a contact 23. Together, the diffused resistor 17 and the field plate diode or traansistor 19 act as an isolation stage between the pad 10 and the internal circuitry of the chip. The node 18 is connected to the internal circuitry of the chip (such as an address buffer, etc.) at a metal-to-silicon contact 24. The transistor 19 has the usual thin gate oxide beneath the poly gate 22, whereas the transistor 13 has a thick field oxide beneath its gate 14.

It has been found that a vital feature of the protection circuit of FIGS. 1, 2 and 3 is the channel width W of the transistor 13, and the spacing A between the channel edge 25 and the metal-to-silicon contact 26 connecting the drain 12 to the connector 11. The reason for criticality of this spacing A is due to the heat generated in the channel area of transistor 13, and the fact that this heat travels along the surface of the silicon from the edge 25 to the metal contact 26, melts the aluminum of this contact, which in turn penetrates the silicon by alloying, and shorts the junction. Since silicon is a good heat conductor compared to silicon oxide, the path is along the surface to the contact rather than vertically to the metal above the junction.

The input protection circuit of FIGS. 1, 2 and 3 is designed to withstand electrostatic voltage build-up of, for example, seven or eight thousand volts on the pad 10. An electrostatic voltage is discharged by a very rapid current spike with very high peak current but short duration. Ordinarily, MOS devices will withstand only about 3000 volts. Voltages of this magnitude are easily generated by friction in routine handling, so special precautions have been needed to keep all of the terminals grounded or shorted together to avoid damage due to these electrostatic voltages.

In accordance with the invention, the channel width W of the transistor 13 is at least about five or six mils so that it can conduct a large instantaneous current spike with low forward drop. The channel length is about 3 microns, but this is not critical; usually the channel length is the same as the standard channel length for most transistors for the design rules used for the particular chip design. The distance A is more critical. This is selected to be at least about six or seven microns, preferably eight or ten, whereas for 3-micron design rules the spacing would ordinarily be about three microns. Thus, the spacing A is about two or three times what would usually be expected. This spacing A, according to the invention, increases the electrostatic discharge protection from about 3000 v to at least double that level, or triple. It has been found that a monotonically increasing relationship exists for spacing A, and a linear relationship exists for width W, vs. the allowable ESD level, up

to about 9 or 10000 v, at which point another failure mechanism takes over.

The device of FIGS. **1**, **2** and **3** is constructed by the standard N-channel silicon gate MOS process such as that disclosed in U.S. Pat. No. 4,055,444, issued to G. R. Mohan Rao, assigned to Texas Instruments.

Referring to FIGS. **4**, **5** and **6**, the concept of the invention can be applied as well to output terminals. An output bonding pad **30** is connected by a metal line **31** to the drain **32** of a transistor **33** which has its source **34** connected to Vss line **35**. On the high side the metal line **31** is connected to the source **36** of a transistor **37** which has its drain **38** connected to a Vdd line **39**. The gates **40** and **41** of these two transistors **33** and **37** are driven by complementary signals, providing a push-pull output. These two transistors are ordinarily of interdigitated structure to provide uniform current density at high current capacities. Only one small part of the transistor structure is shown in FIGS. **5** and **6**. The effective channel width W of each of the transistors **33** and **37** is over 400 microns (broken into segments), for example, and so these can withstand a substantial current spike caused by ESD. However, the problem of melted aluminum at contact areas **42** and **43** would still exist. For this reason, the spacing A is greater than what would ordinarily be expected, as discussed above, so that the heat generated in the channel beneath the gate **40** or **41** does not reach the aluminum contact within the time the current spike subsists.

A CMOS circuit can also use the features of the invention. Usually an input protection circuit for CMOS devices employs a pair of diodes instead of the thick oxide transistor **13**, one diode going to Vss and the other to Vdd. The heat-generating part of a diode is depletion region of the junction, as in a transistor. Thus, the critical spacing is the distance between the metal-to-silicon contact engaging one electrode of the diode, and the junction of the diode. To provide a high level of ESD protection, this spacing should be about two or three times the "design rule" spacing. Preferably, this spacing should be five or six microns or more to achieve in excess of 7000 or 8000 volts ESD immunity.

While this invention has been described with reference to an illustrative embodiment, this description is not intended to be construed in a limiting sense. Various modifications to the illustrative embodiment, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

What is claimed is:

1. An input protection structure for an MOS device, comprising:

(a) a metal input pad on a face of a silicon chip,

(b) a transistor having a thick gate oxide, having a source-to-drain path connecting said metal input pad to a voltage-supply conductor, having a metal gate, and having a drain region directly connected to said metal gate and metal input pad at an elongated contact area parallel to the width of said source-to-drain path,

(c) wherein the width of said source-to-drain path is at least about 25 times the length of the source-to-drain path, and wherein the spacing along said face between said source-to-drain path and said elongated contact area is at least about twice said length of the source-to-drain path.

2. A structure according to claim **1** wherein said metal gate is an extended area of said metal input pad.

3. A structure according to claim **2** wherein said transistor has a source region in said face, said voltage supply conductor is a metal line running along said face and ordinarily connected to ground, and a metal-to-silicon contact area connects said metal line to said source region, said metal-to-silicon contact area also being spaced from said source-to-drain path by at least about twice said length of the source-to-drain path.

4. A protection structure for a semiconductor device, comprising:

(a) a metal bonding pad at a face of a silicon chip,

(b) a current path in said face of the silicon chip at the surface thereof, said current path being many times wider than its length;

(c) means at said face including a metal-to-silicon contact area directly connected to said metal bonding pad without intervening resistor devices, said means coupling said current path in series between said metal bonding pad and a voltage supply terminal of said chip,

(d) said contact area extending along the face parallel to the width dimension of said current path, for at least a substantial part of the width thereof, said contact area being spaced from said current path by an amount at least about twice the length of the current path.

5. A structure according to claim **4** wherein said current path is the channel of an MOS transistor.

6. A structure according to claim **5** wherein said metal contact is integral with a metal gate of said transistor extending over said channel.

7. A structure according to claim **6** wherein said metal contact is integral with said metal bonding pad.

8. A structure according to claim **5** wherein said channel is segmented and the transistor has interdigitated source and drain regions.

9. A structure according to claim **8** wherein said bonding pad is an output terminal.

10. A structure according to claim **4** wherein said current path is at a PN junction.

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